FIG.1

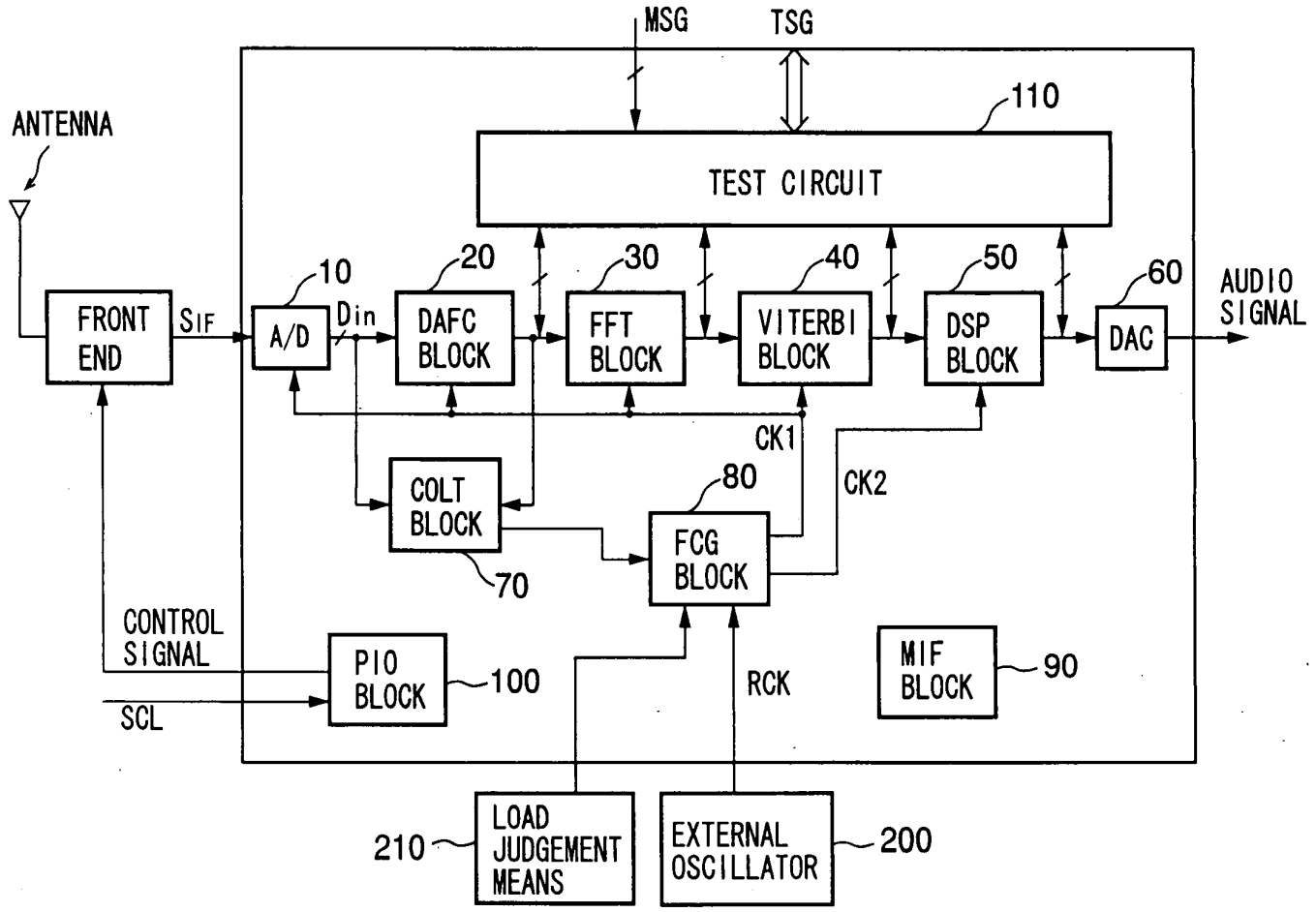

MSG
TSG
110
TEST CIRCUIT
ANTENNA
FRONT END
SIF
A/D
10
Din
DAFC BLOCK
20
FFT BLOCK
30
VITERBI BLOCK
40
DSP BLOCK
50
DAC
60
AUDIO SIGNAL
CK1
CK2
COLT BLOCK
70
FCG BLOCK
80
CONTROL SIGNAL
SCL
PIO BLOCK
100
RCK
MIF BLOCK
90
210
LOAD JUDGEMENT MEANS
EXTERNAL OSCILLATOR
200

FIG.2

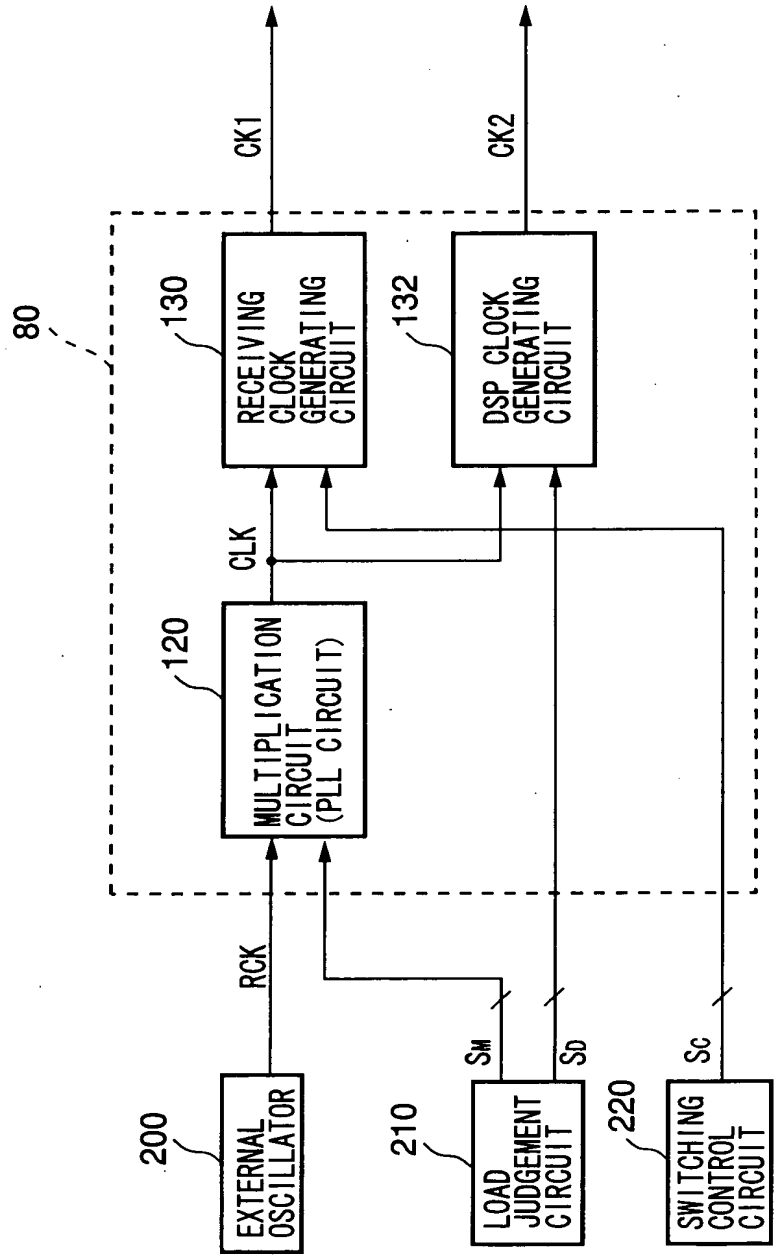

80
CK1
CK2
130
RECEIVING CLOCK GENERATING CIRCUIT
132
DSP CLOCK GENERATING CIRCUIT
CLK
120
MULTIPLICATION CIRCUIT (PLL CIRCUIT)
RCK
200
EXTERNAL OSCILLATOR
SM
SD
210
LOAD JUDGEMENT CIRCUIT
SC
220
SWITCHING CONTROL CIRCUIT

FIG.3

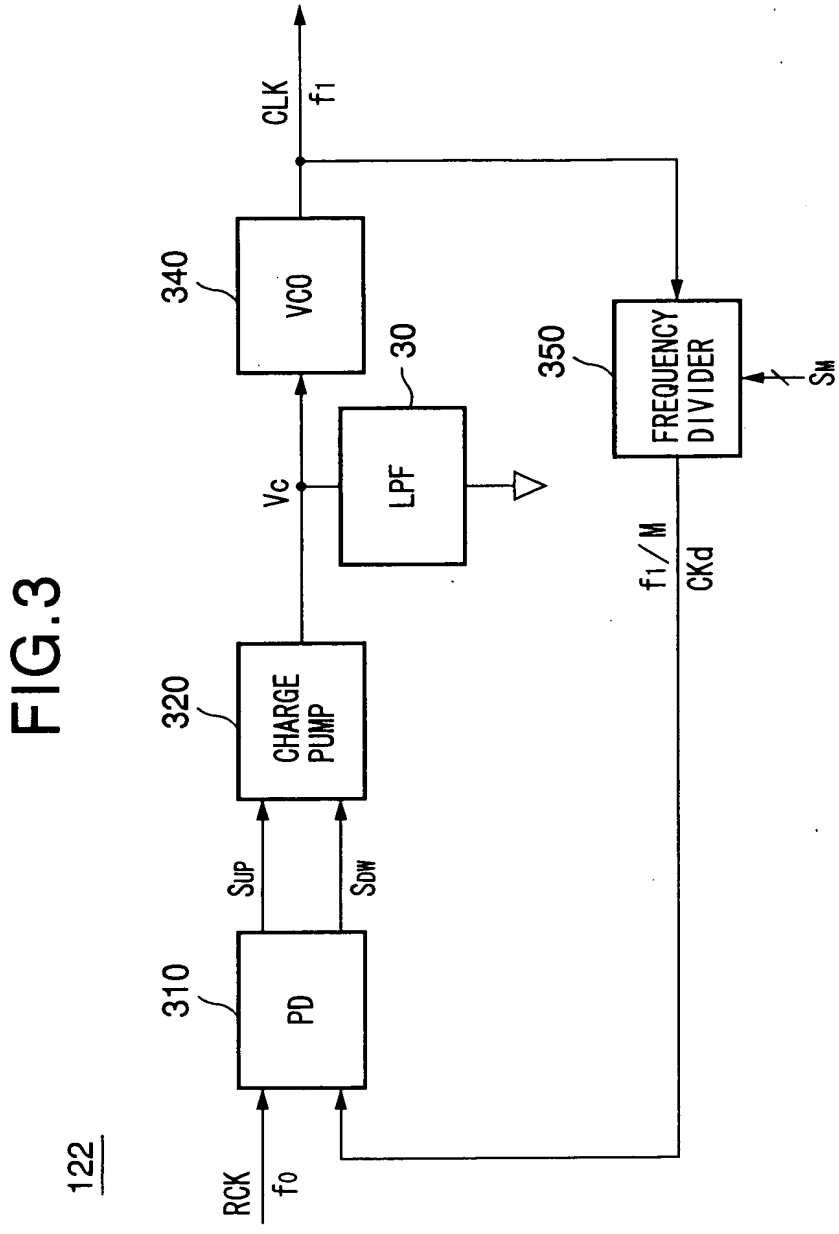

122
RCK
f0
310
PD
SUP
SDW
320
CHARGE PUMP
Vc
LPF
30
340
VCO
CLK
f1
350
FREQUENCY DIVIDER
SM
f1/M
CKd

FIG.4A RCK (24.576MHz)

FIG.4B CLK (98.304MHz)

FIG.4C CK1 (24.576MHz) (FREQUENCY DIVISION RATIO N=4)

FIG.4D CK2 (49.152MHz) (FREQUENCY DIVISION RATIO N=2)

FIG.4E CK2 (24.576MHz) (FREQUENCY DIVISION RATIO N=4)

FIG.4F CK2 (12.288MHz) (FREQUENCY DIVISION RATIO N=8)

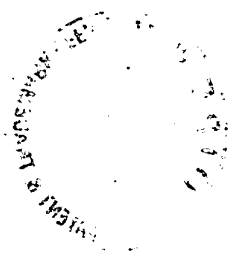


FIG.5

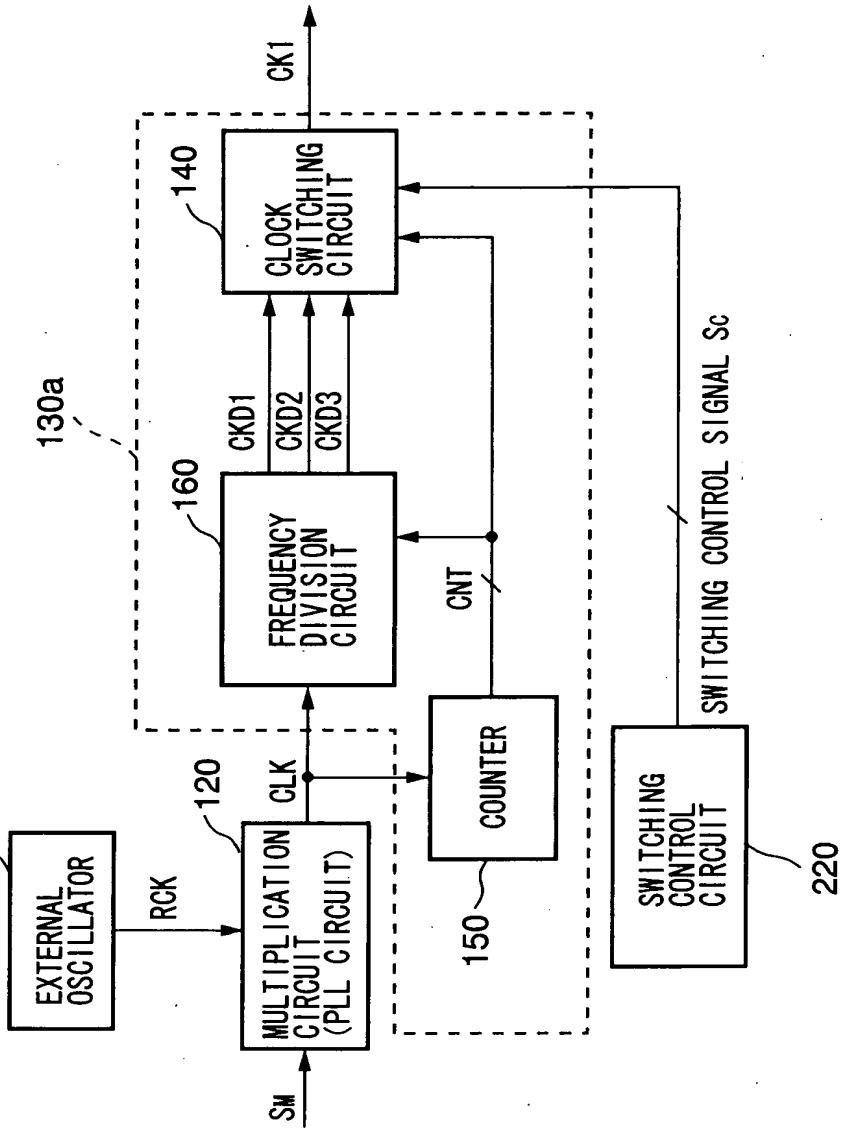

200
EXTERNAL OSCILLATOR
RCK
120
MULTIPLICATION CIRCUIT (PLL CIRCUIT)
SM
CLK
130a
160
FREQUENCY DIVISION CIRCUIT
CKD1
CKD2
CKD3
140
CLOCK SWITCHING CIRCUIT
CK1
CNT
150
COUNTER
SWITCHING CONTROL SIGNAL Sc
SWITCHING CONTROL CIRCUIT
220

FIG.6

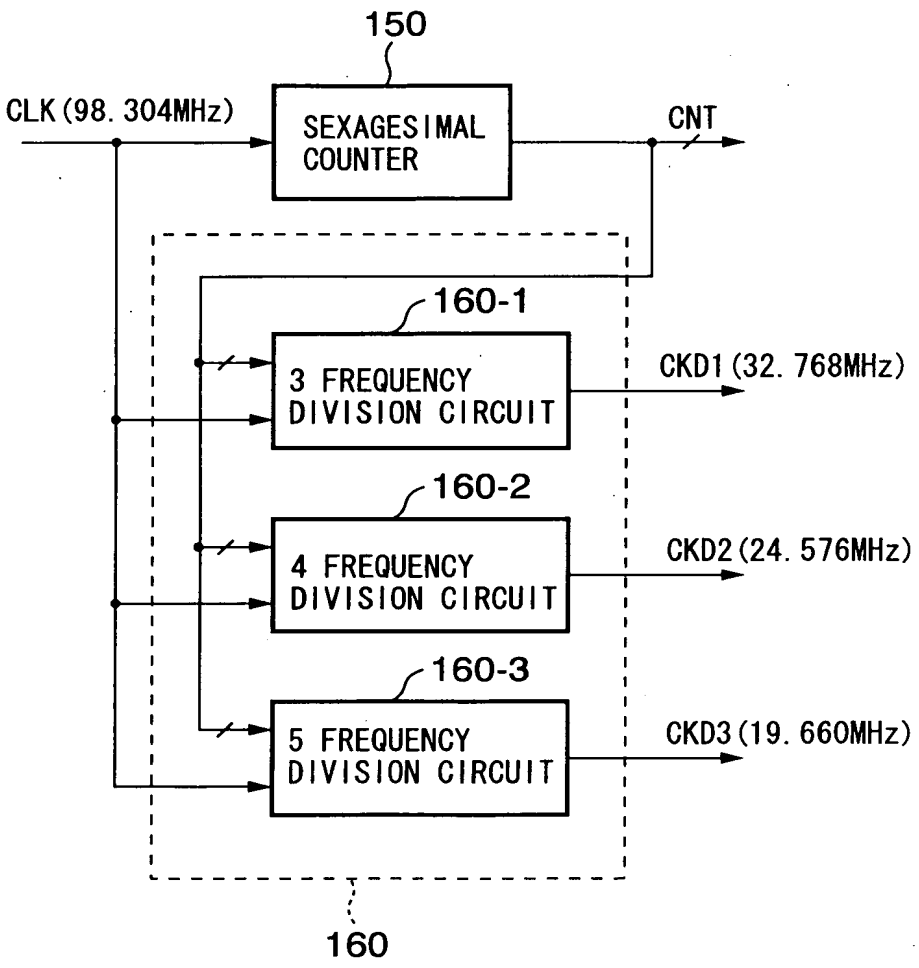

150
CLK (98.304MHz)
SEXAGESIMAL COUNTER
CNT
160-1
3 FREQUENCY DIVISION CIRCUIT
CKD1 (32.768MHz)
160-2
4 FREQUENCY DIVISION CIRCUIT
CKD2 (24.576MHz)
160-3
5 FREQUENCY DIVISION CIRCUIT
CKD3 (19.660MHz)
160

FIG.7

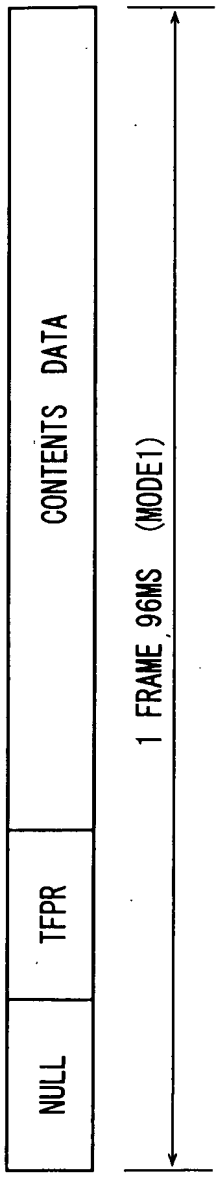


FIG.8

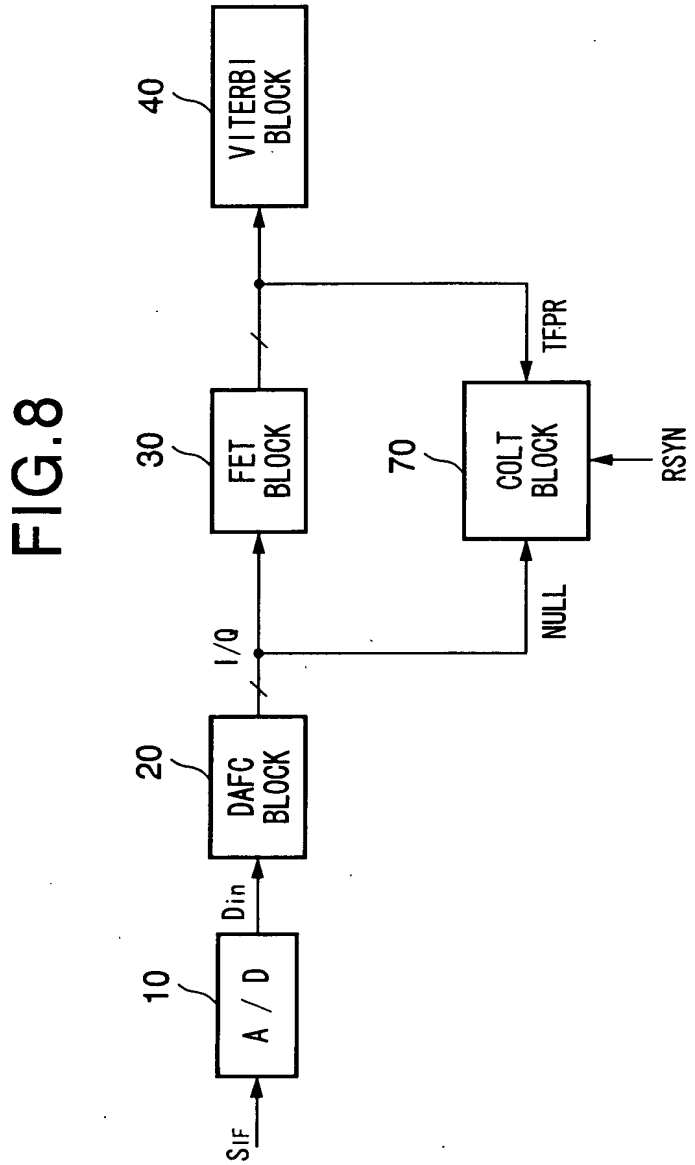
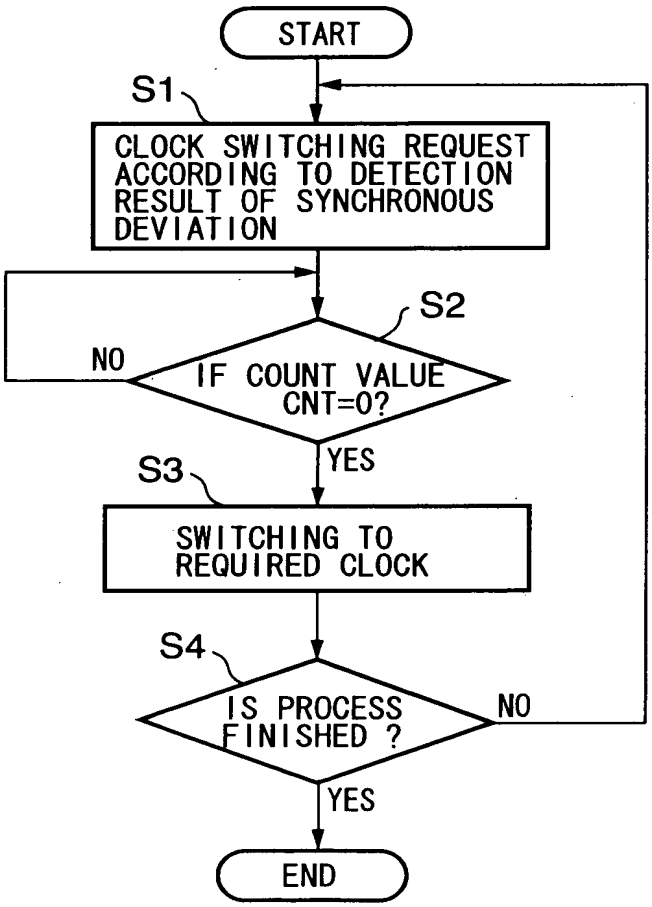

10
A / D
Din
20
DAFC BLOCK
I/Q
30
FET BLOCK
40
VITERBI BLOCK
70
COLT BLOCK
TFPR
NULL
RSYN
SIF

FIG.9


START
S1
CLOCK SWITCHING REQUEST ACCORDING TO DETECTION RESULT OF SYNCHRONOUS DEVIATION
S2
NO
IF COUNT VALUE CNT=0?
YES
S3
SWITCHING TO REQUIRED CLOCK
S4
IS PROCESS FINISHED ?
NO
YES
END

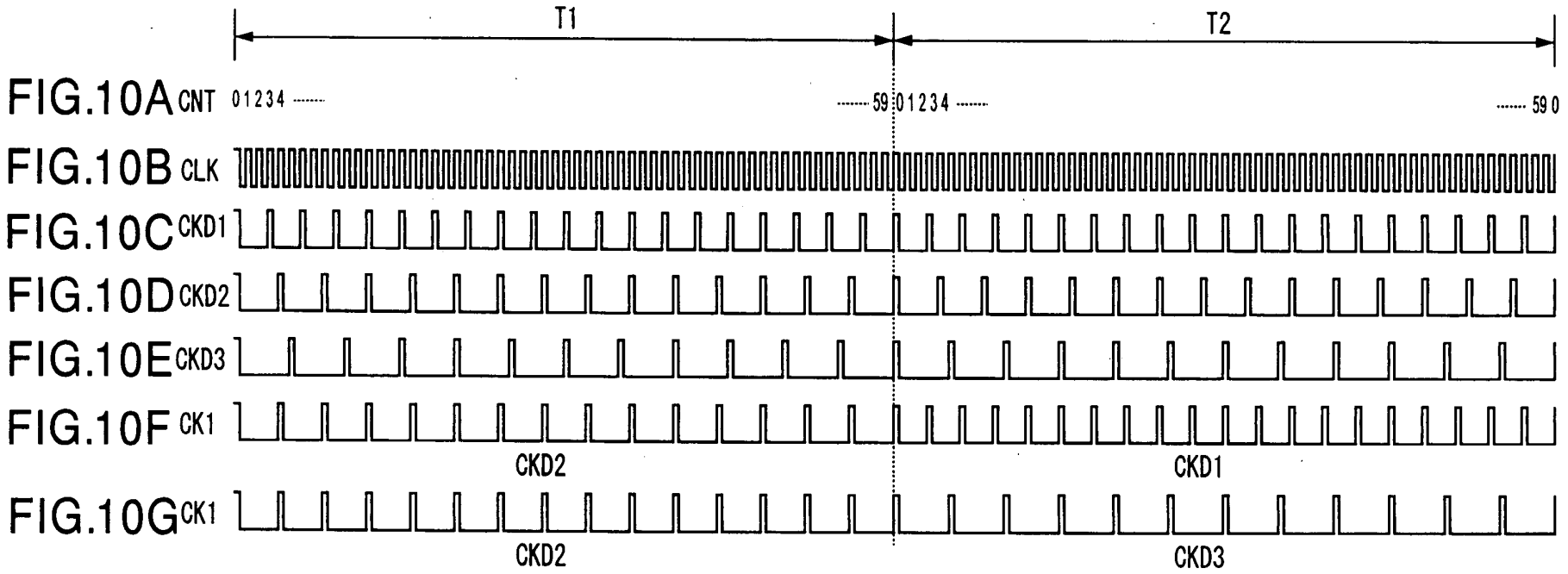

T1
T2
FIG.10A CNT
01234 ..... 59 01234 590
FIG.10B CLK
FIG.10C CKD1
FIG.10D CKD2
FIG.10E CKD3
FIG.10F CK1
CKD2
CKD1
FIG.10G CK1
CKD2
CKD3

FIG.11

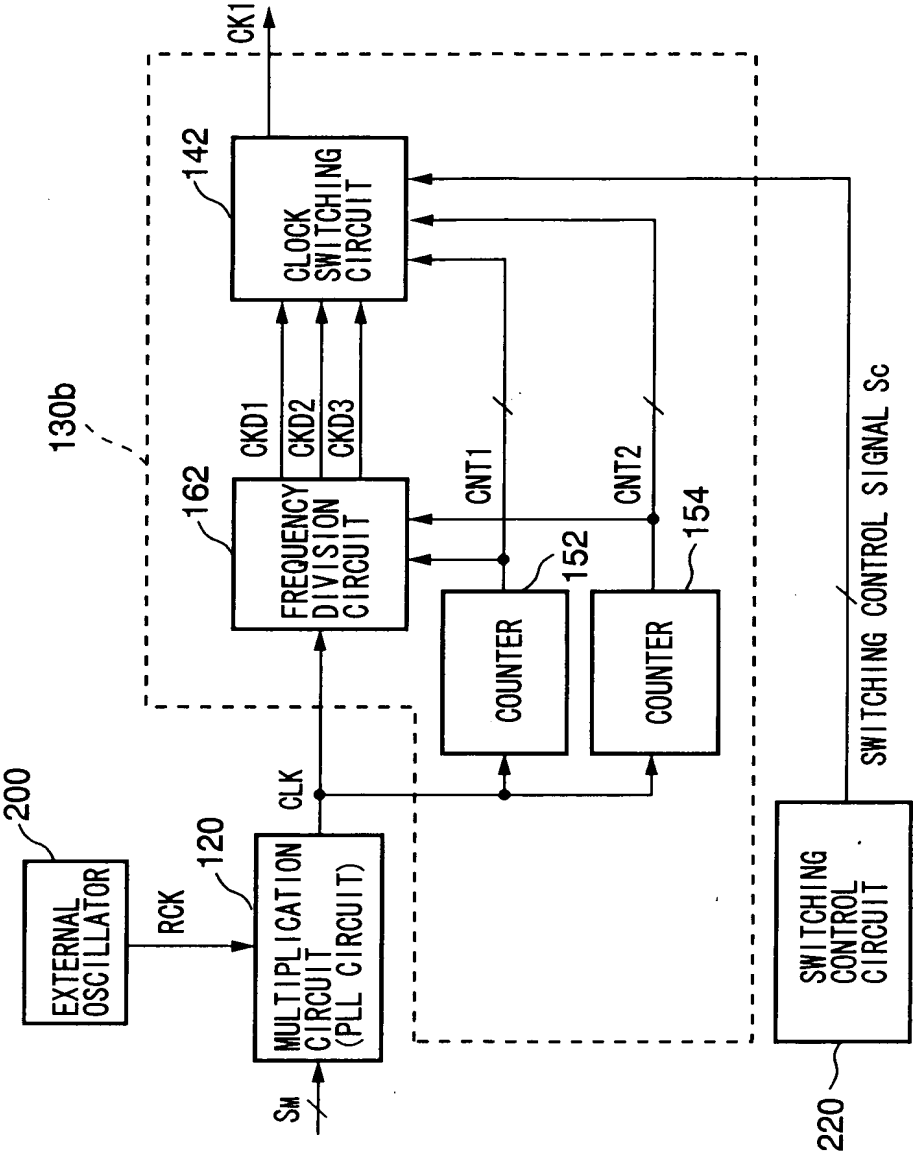

CK1
142
CLOCK SWITCHING CIRCUIT
130b
CKD1
CKD2
CKD3
162
FREQUENCY DIVISION CIRCUIT
CNT1
CNT2
152
154
COUNTER
COUNTER
SWITCHING CONTROL SIGNAL Sc
200
EXTERNAL OSCILLATOR
RCK
120
MULTIPLICATION CIRCUIT (PLL CIRCUIT)
CLK
SM
SWITCHING CONTROL CIRCUIT
220

FIG.12

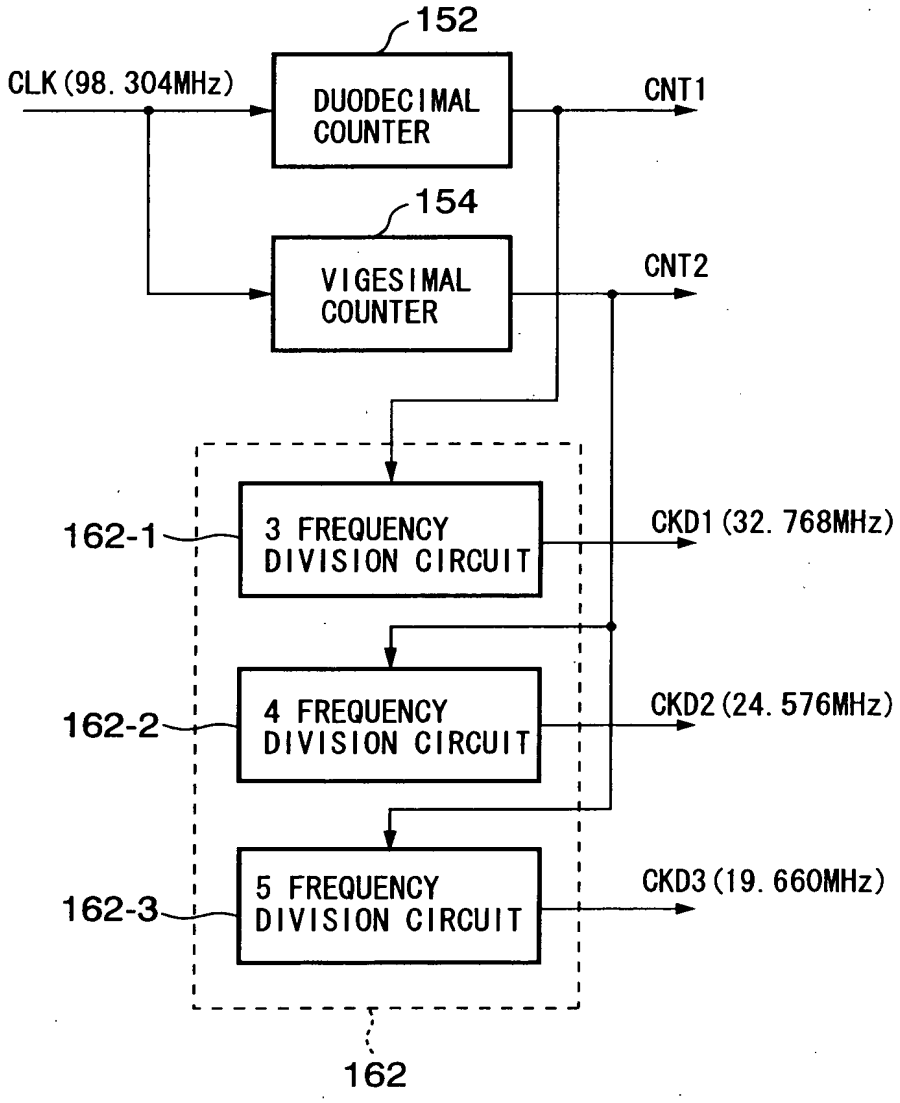

152
CLK (98.304MHz)
DUODECIMAL COUNTER
CNT1
154
VIGESIMAL COUNTER
CNT2
162-1
3 FREQUENCY DIVISION CIRCUIT
CKD1 (32.768MHz)
162-2
4 FREQUENCY DIVISION CIRCUIT
CKD2 (24.576MHz)
162-3
5 FREQUENCY DIVISION CIRCUIT
CKD3 (19.660MHz)
162

FIG.13

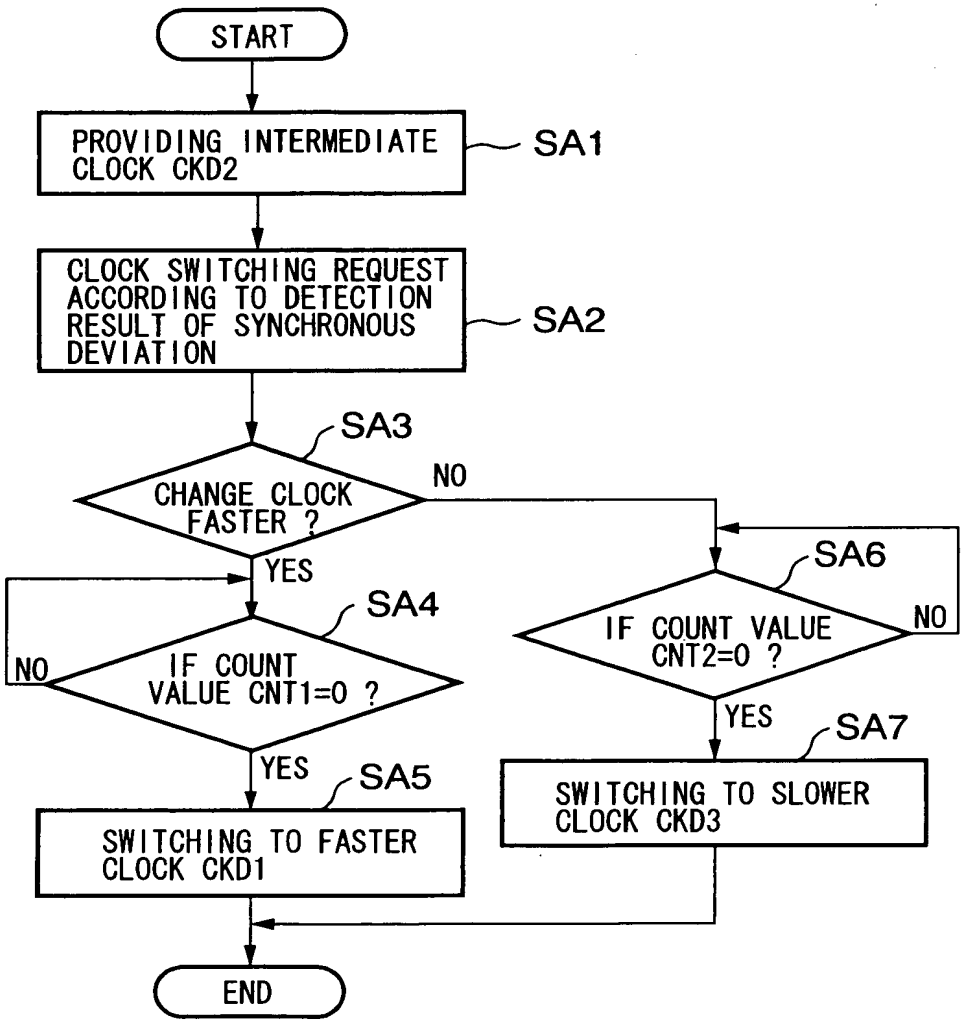

START
PROVIDING INTERMEDIATE CLOCK CKD2
SA1
CLOCK SWITCHING REQUEST ACCORDING TO DETECTION RESULT OF SYNCHRONOUS DEVIATION
SA2
SA3
CHANGE CLOCK FASTER ?
NO
YES
SA4
NO
IF COUNT VALUE CNT1=0 ?
YES
SA5
SWITCHING TO FASTER CLOCK CKD1
SA6
IF COUNT VALUE CNT2=0 ?
NO
YES
SA7
SWITCHING TO SLOWER CLOCK CKD3
END

FIG.14

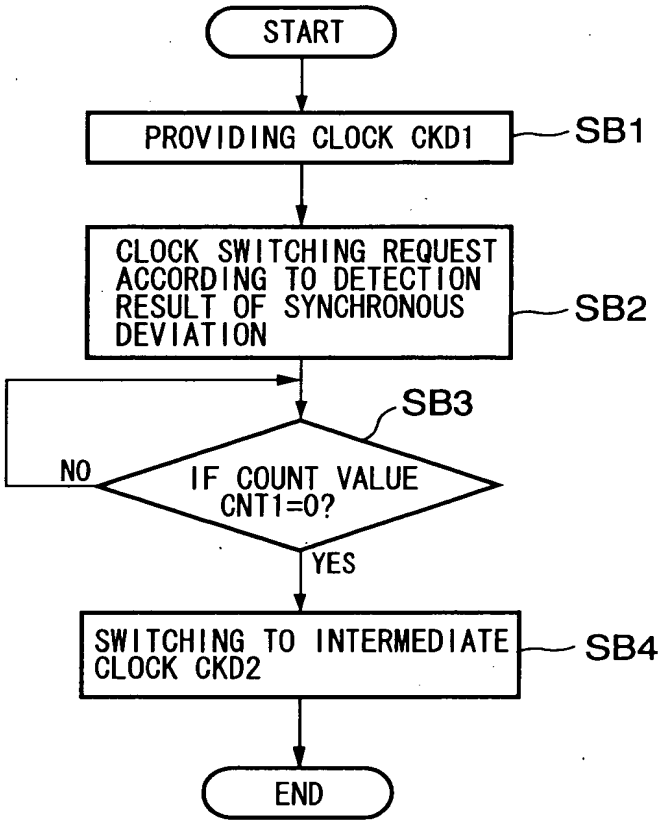
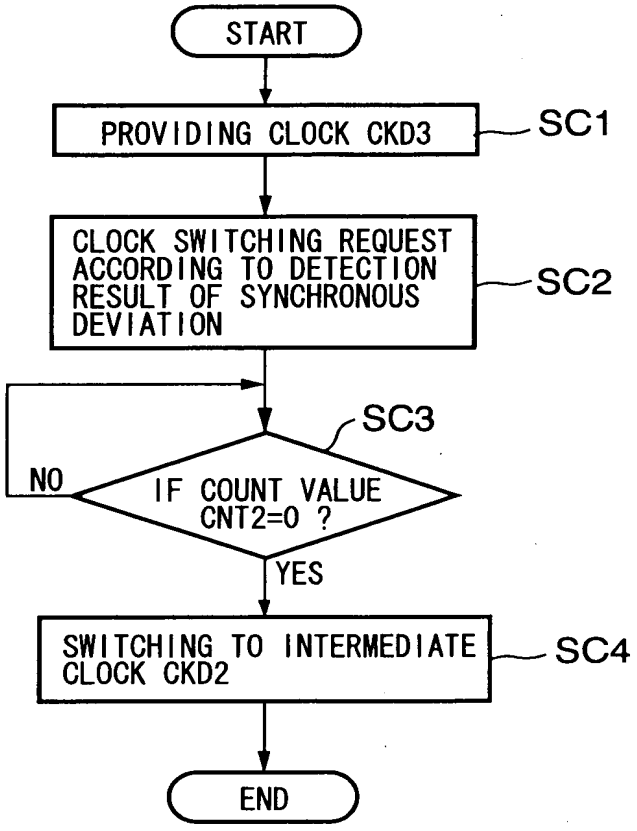

START
PROVIDING CLOCK CKD1
SB1
CLOCK SWITCHING REQUEST ACCORDING TO DETECTION RESULT OF SYNCHRONOUS DEVIATION
SB2
SB3
NO
IF COUNT VALUE CNT1=0?
YES
SWITCHING TO INTERMEDIATE CLOCK CKD2
SB4
END

FIG.15


START
PROVIDING CLOCK CKD3
SC1
CLOCK SWITCHING REQUEST ACCORDING TO DETECTION RESULT OF SYNCHRONOUS DEVIATION
SC2
SC3
NO
IF COUNT VALUE CNT2=0 ?
YES
SWITCHING TO INTERMEDIATE CLOCK CKD2
SC4
END

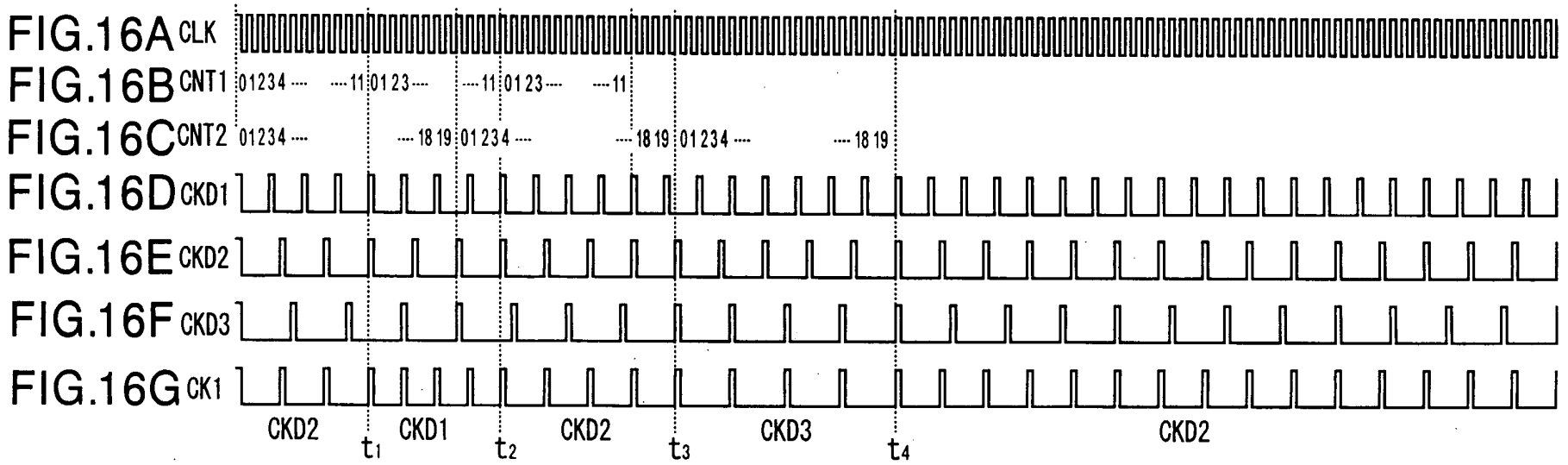


FIG.16A CLK
FIG.16B CNT1
FIG.16C CNT2
FIG.16D CKD1
FIG.16E CKD2
FIG.16F CKD3
FIG.16G CK1
01234 ···· ···· 11 01 23 ···· ···· 11 01 23 ···· ···· 11
01234 ···· ···· 18 19 01 234 ···· ···· 18 19 01 234 ···· ···· 18 19
CKD2
CKD1
CKD2
CKD3
CKD2
t1
t2
t3
t4

FIG.17

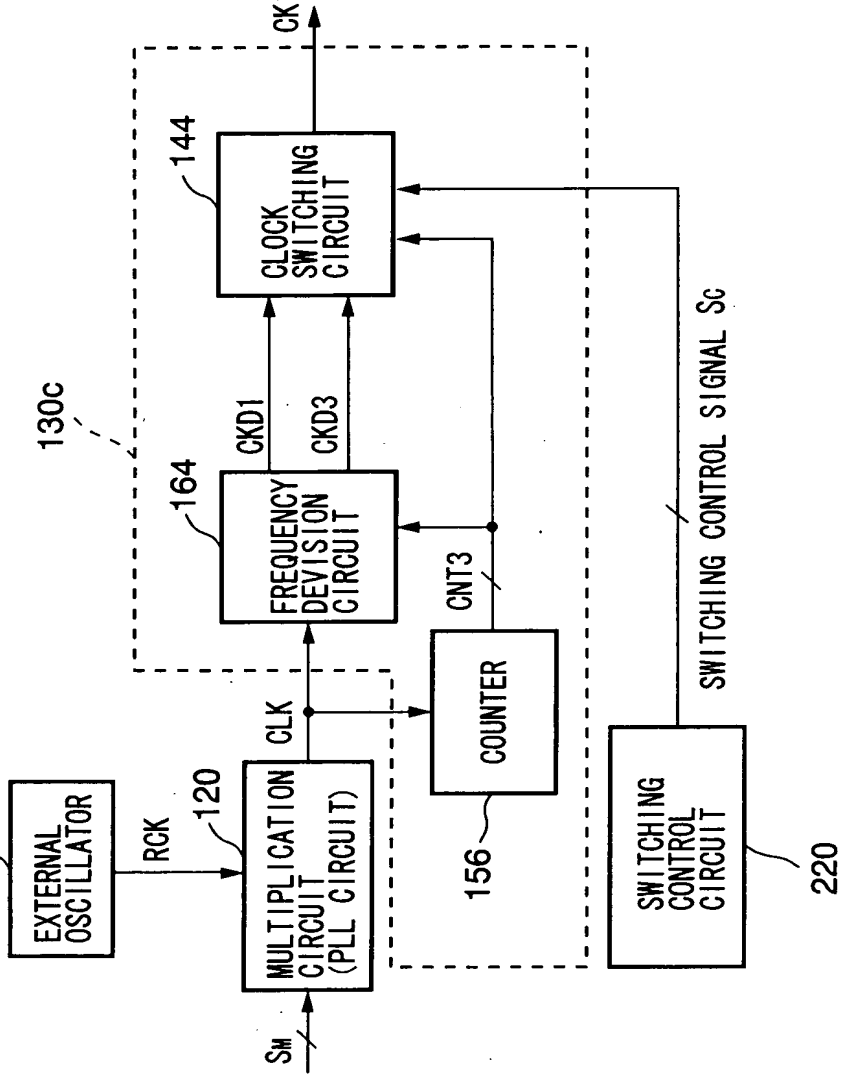

CK1
144
CLOCK SWITCHING CIRCUIT
130c
CKD1
CKD3
164
FREQUENCY DEVISION CIRCUIT
CNT3
COUNTER
156
CLK
200
EXTERNAL OSCILLATOR
RCK
120
MULTIPLICATION CIRCUIT (PLL CIRCUIT)
Sm
SWITCHING CONTROL SIGNAL Sc
SWITCHING CONTROL CIRCUIT
220

FIG.18

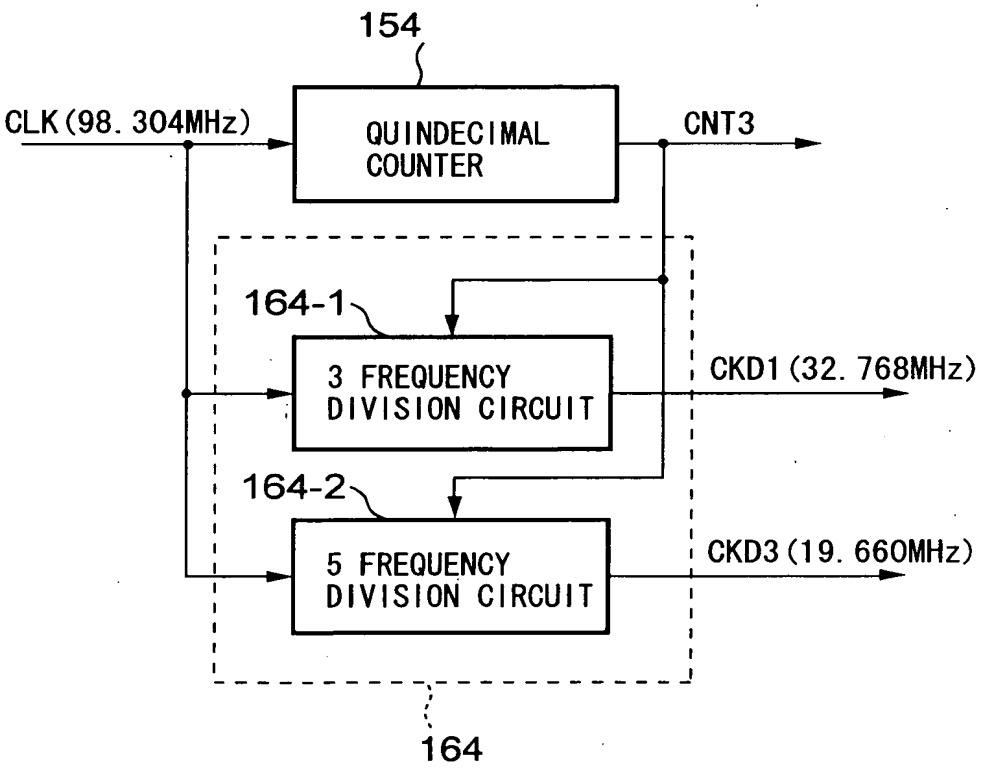
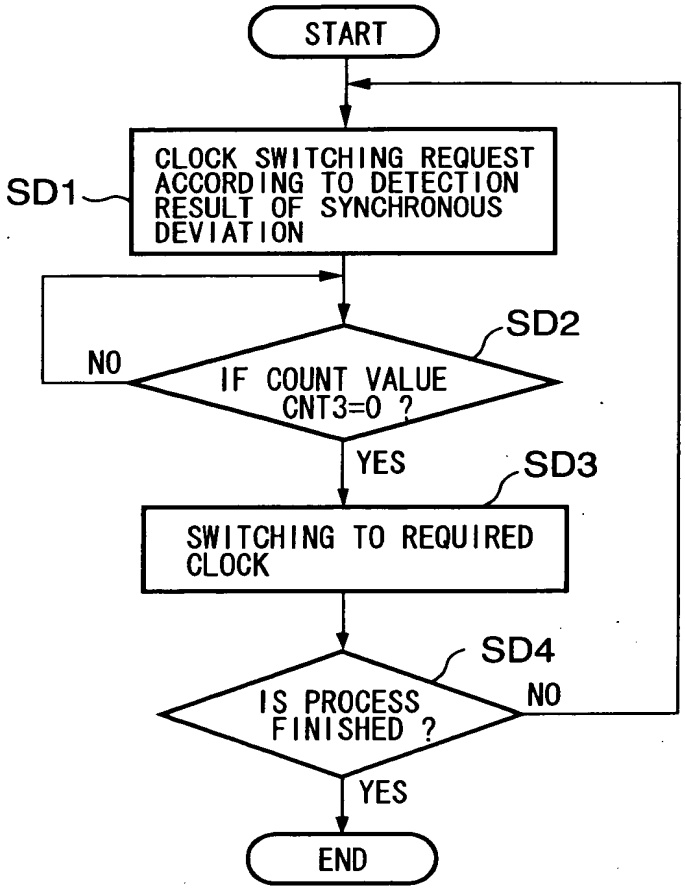
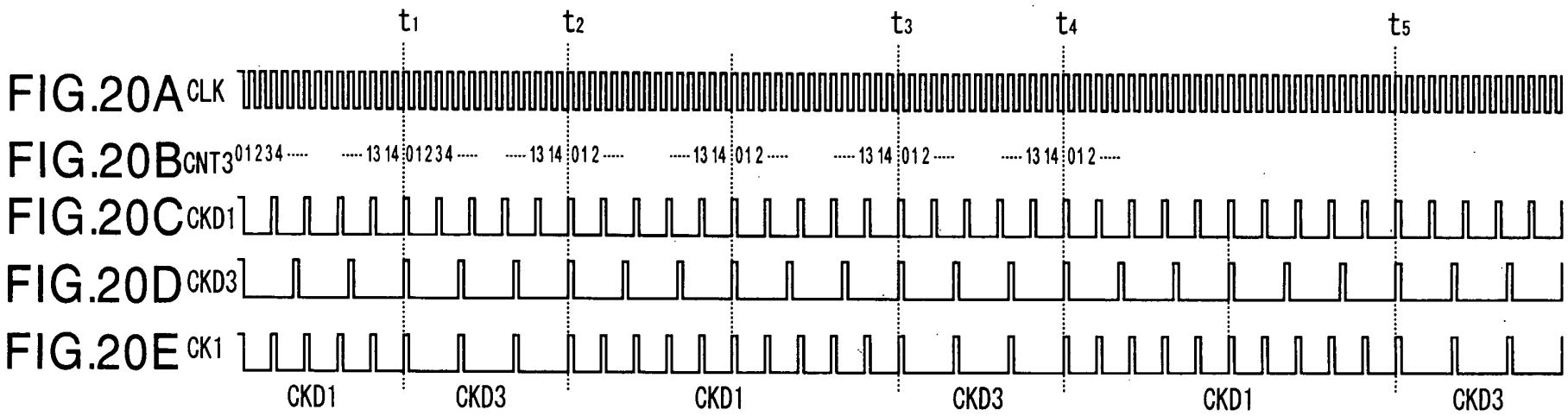

154
CLK (98.304MHz)
QUINDECIMAL COUNTER
CNT3
164-1
3 FREQUENCY DIVISION CIRCUIT
CKD1 (32.768MHz)
164-2
5 FREQUENCY DIVISION CIRCUIT
CKD3 (19.660MHz)
164

FIG.19


START
CLOCK SWITCHING REQUEST ACCORDING TO DETECTION RESULT OF SYNCHRONOUS DEVIATION
SD1
SD2
NO
IF COUNT VALUE CNT3=0 ?
YES
SD3
SWITCHING TO REQUIRED CLOCK
SD4
IS PROCESS FINISHED ?
NO
YES
END


t1
t2
t3
t4
t5
FIG.20A CLK
FIG.20B CNT3
FIG.20C CKD1
FIG.20D CKD3
FIG.20E CK1
CKD1
CKD3
CKD1
CKD3
CKD1
CKD3